

Pulse generator

The invention relates to a pulse generator comprising a series coupling of delay elements, every two consecutive delay elements being coupled in a plurality of coupling points, the series coupling of delay elements having a first end and a second end coupled to a first signal and to a second signal, respectively, the signals having a same frequency and being mutually phase-shifted.

Normally a pulse i.e. a binary signal, or a sinusoidal signal, is generated using a reference crystal oscillator and a voltage controlled oscillator (VCO). The crystal oscillator and the VCO are connected in a PLL configuration. When high-speed pulse is necessary, the VCO have to generate high frequency signals. Building a VCO beyond 5 GHz is not a simple task. The main problems are phase noise and tuning range. Hence, pulses having a period of less than 0.2ns are difficult to be generated, certainly when the jitter needs are less than a few pico seconds. The amount of jitter in a PLL is related to the bandwidth of the loop filter included in the PLL. The larger the bandwidth, the lower the jitter. For stability reasons, the loop bandwidth must be a factor 10 lower than the reference clock. Thus a high reference clock frequency is helpful.

US-A-5,838,178 describes a frequency multiplier comprising embodied in a phase-locked loop (PLL). The PLL comprises a plurality of delay elements that furnish successive phase-shifted signals to a logical adder made up by EXCLUSIVE OR (XOR) gates. It is observed that there are necessary at least three level of XOR gates, the total number of XOR gates being at least 7. When integrating on a single chip the gates increase the area used by the PLL and implicitly it's price. It is further observed that there are supplementary delays associated to the XOR gates making precise duration pulse generation hard to be realized. Furthermore, using only digital gates, the signals provided at their inputs have to be binary signals having high slope edges.

It is therefore an object of the present invention to obtain a high frequency pulse generator having a reduced price and a low jitter.

In accordance with the invention this is achieved in a device according to the first paragraph characterized in that it further comprises a zero-crossing detector coupled to two mutually different coupling points for generating an output pulse having a duration determined by a ratio between a number of delay elements between the two different coupling points and a total delay of the series coupling of delay elements. The total delay through the delay elements considering that to each delay element D_i corresponds a

respective delay d_i is $\text{Delay} = \sum_{i=1}^N d_i$. A phase-shift φ_i corresponds to a respective delay d_i .

Let us consider that the total phase-shift between the first signal and the second signal is Φ . Hence the phase-shift associated to a delay element D_i is φ_i/Φ . It is convenient to relate these delays to a well-defined amplitude level of the signals and a convenient level is the zero voltage level, considering that the signals amplitudes are between + and - same voltage i.e. the signal is bipolar. If the signal is unipolar, it could be used a level corresponding to an average voltage between a maximum one and a minimum one.

In an embodiment of the invention an oscillator coupled to a phase-shifter generates the first signal and the second signal. A relative simple way to generate phase-shifted signals is a coupling between an oscillator and a phase-shifter. The phase-shifter provides a signal having a frequency substantially equal to the frequency of the signal generated by the oscillator and mutually phase-shifted. A value of the phase-shift determines the necessary number for the delay elements for generating a pulse having a specified duration. It is pointed out that whenever a quadrature oscillator is available, as in modern communication systems, the first and the second signals could be the in-phase and the quadrature signals generated by the oscillator. Hence, a further cost and complexity reductions are obtained.

In another embodiment of the invention the delay elements comprise equal-value resistor means. Resistor means are very suitable to be used as delay elements because they do not introduce additional phase-shifts and consequently no additional parasitic delays. Furthermore, using nowadays technology it is possible to integrate very high precision resistors and therefore to obtain substantially equal-value delays.

In another embodiment of the invention the zero-crossing detector is a latch. As it is well known, latches are bi-stable devices that are used in digital sequential circuit design. Whenever the first signal is bigger than zero the latch generates a logical 1 and when

the second signal is bigger than zero the latch generates a logical zero. It is first observed that the pulse could be also generated using complementary input signals. Additionally, the output pulse could be also complementary to the above-mentioned situation. In fact there are possible multiple possible combinations for obtaining the output pulse using a latch, the combinations being obvious for a skilled person in the art.

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The above and other features and advantages of the invention will be apparent from the following description of exemplary embodiments of the invention with reference to 10 the following drawings, in which:

Fig. 1 depicts a pulse generator according to the invention,

Fig. 2 depicts an embodiment of the pulse generator using quadrature signals and resistors, and

Fig. 3 depicts the In-phase and Q-phase signals generated by a quadrature

15 oscillator.

Fig. 1 depicts a pulse generator according to the invention. The pulse generator comprises a series coupling of delay elements D1, D2, D3, D4, D5. Every two consecutive delay elements D1, D2, D3, D4, D5 are coupled to each other in a plurality of coupling points A1, A2, A3, A4. The series coupling of delay elements D1, D2, D3, D4, D5 has a first end A0 and a second end A5 coupled to a first signal y and a second signal , respectively. The signals x, y have a same frequency and are mutually phase-shifted. The pulse generator further comprises a zero-crossing detector 3 coupled to two different coupling points A2, A3 and generating an output pulse O having a duration determined by a ratio between a number of delay elements between the two different coupling points and a total delay of the series coupling of delay elements. Considering that to each delay element Di corresponds a respective delay di, the total delay through the delay elements is Delay =

$$\sum_{i=1}^N di .$$
 A phase-shift φ_i corresponds to a respective delay di. Let us consider that the total

30 phase-shift between the first signal and the second signal is Φ . Hence the phase-shift associated to a delay element Di is φ_i/Φ . It is convenient to relate these delays to a well-defined amplitude level of the signals and a convenient level is the zero voltage level, considering that the signals amplitudes are between + and - same voltage i.e. the signal is

bipolar. If the signal is unipolar, it could be used a level corresponding to an average voltage between a maximum one and a minimum one. The signals x, y are generated by an oscillator 1 coupled to a phase shifter 2, respectively.

5 The mechanism of generation of relatively high frequency pulse is discussed using Fig. 2, which depicts an embodiment of the pulse generator using quadrature signals and resistors. Resistors are very suitable to be used as delay elements because they do not introduce additional phase-shifts and consequently no additional parasitic delays. Furthermore, using nowadays technology it is possible to integrate very high precision resistors and therefore to obtain substantially equal-value delays.

10 Furthermore let us consider that all the resistors have a substantially equal value and, therefore, they provide substantially equal delays. In addition to this we propose the following concept. Suppose we have a quadrature oscillator 10, generating a sinusoidal signal having a frequency equal to 1 GHz. For such frequency, relatively low phase noise can be obtained (-140 dBc at 1 MHz offset), the oscillator having a relatively large tuning range 15 (2:1 or more). For a 1 GHz signal, the zero crossings of any of the sinusoidal output signals I and Q are separated by 0.5ns. Considering the I signal as reference then the Q signal is 0.25ns delayed compared to the signal I because the signals are in quadrature. Because the delay elements are equal valued, it results that the zero crossing at resistor connected between A0 and A1 is delayed by 0.05ns compared to the I-signal and the zero crossing at resistor 20 connected between A1 and A2 is delayed 0.1ns. In Fig. 3 the I/Q signal and the intermediate signals are plotted. In general, for n identical resistors, we have at node j a delay time that equals 0.25ns/n*j compared to the I-signal and the delay between to adjacent resistors is 0.05ns or 0.25ns/n in general for n resistors. We can use the zero crossing to drive a fast latch to generate the pulse. If the adjacent resistors are used, the pulse is 0.05ns or 20 GHz, if the I 25 and Q signals are sinusoidal signals of 1 GHz. In Fig. 2 a latch 30 is coupled to two consecutive connection points A2 and A3 between the resistors. Whenever the signal Q is bigger that zero the latch generates a logical 1 and when the signal I is bigger than zero the latch generates a logical zero. It is first observed that the pulse could be also generated using complementary input signals i.e. signals less than zero when bipolar signals are considered. 30 Additionally, the output pulse could be also complementary to the above-mentioned situation. In fact there are possible multiple possible combinations for obtaining the output pulse using a latch, the combinations being obvious for a skilled person in the art.

From experiments it is known that the noise introduced by latch, up to a frequency of 10 GHz is much less than the quadrature oscillator 10 and therefore will not

influence the zero crossings. Therefore, in this case it is possible to generate accurate 0.1ns pulses from an oscillator 10 providing an output signal having a frequency of 1 GHz. It could be considered that the quadrature oscillator 10 that could be voltage controlled is locked in a Phase Locked Loop to keep the phase noise low and therefore the jitter of the output pulse.

5 The resistors in Fig. 2 should match to each other. Currently, 14 bit accuracy is possible for a ladder of 18 resistors. However, in Fig. 2 only 5 resistors are used.

Let us suppose that the mismatch in the resistors causes an amplitude error:

$$\Delta A = 2A\pi f_i \cdot \Delta t . \quad (1)$$

In relation (1) it is assumed that the oscillator 10 generates a sinusoidal signal having an

10 amplitude A and a frequency f_i . The amplitude error that is related to the mismatch, could be expressed as:

$$\frac{\Delta A}{A} = 2^{-B} \quad (2)$$

where B is number of bits in accuracy. Therefore, the delay error could be expressed as in relation (3)

$$15 \quad \Delta t_{\max} = \frac{2^{-B}}{\pi f_i} \quad (3)$$

As an example, let us consider a precision of 10 bits of the resistors match and that the oscillator 10 generates a quadrature signal I, Q having 1GHz frequency. It results that for the 100ps pulse over the 5-resistor ladder, the frequency f_i is 10GHz. Consequently, the time error due to mismatch is then found is 0.03ps, which is better than the acceptable accuracy
20 for the 100ps pulse.

In principle this technique can be used where fast and accurate pulses are needed. A new principle for wireless communication is under development, named Ultra-wide band communication. In this concept, the information is in the time domain rather than in the frequency domain. A pulse of 10MHz is generated and the data is modulated on this
25 pulse in an exact time frame. To generate this time frame a pulse accuracy of 1ps is needed, which can easily be obtained from the above example. However, this is not trivially obtained from a commercial crystal, which has normally an accuracy of 3-6ps.

It is remarked that the scope of protection of the invention is not restricted to the embodiments described herein. Neither is the scope of protection of the invention
30 restricted by the reference numerals in the claims. The word 'comprising' does not exclude other parts than those mentioned in the claims. The word 'a(n)' preceding an element does not exclude a plurality of those elements. Means forming part of the invention may both be

implemented in the form of dedicated hardware or in the form of a programmed purpose processor. The invention resides in each new feature or combination of features.